

FIG.1

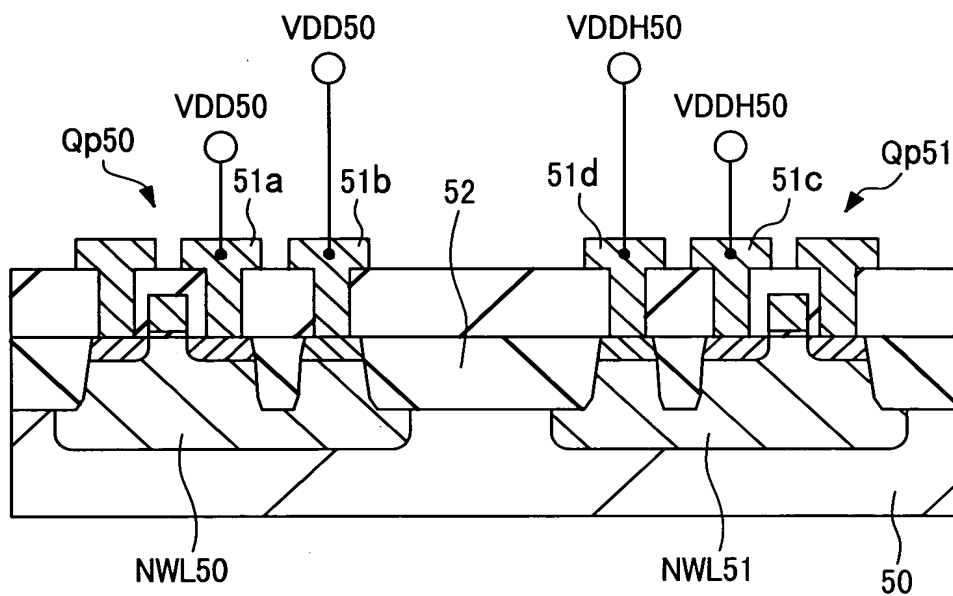


FIG.2

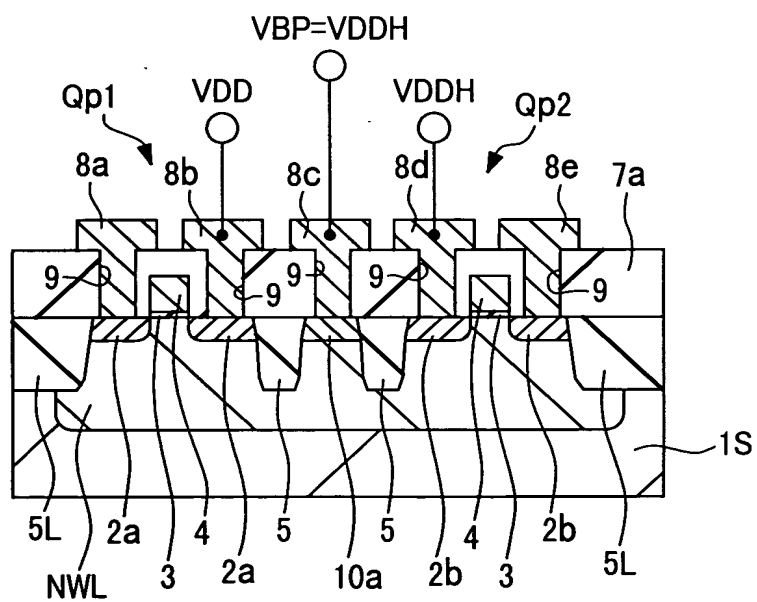


FIG.3

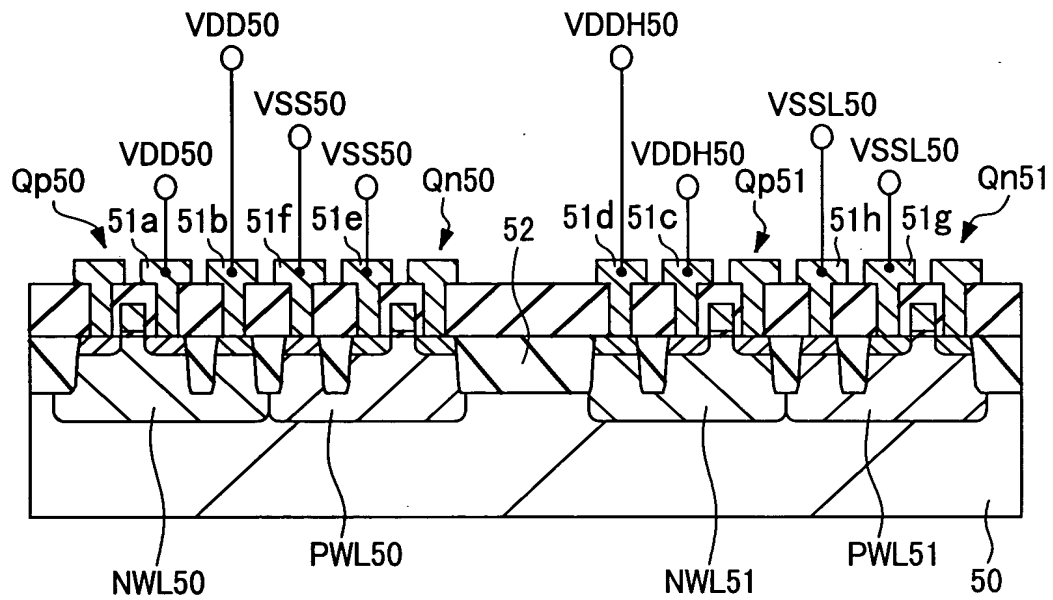
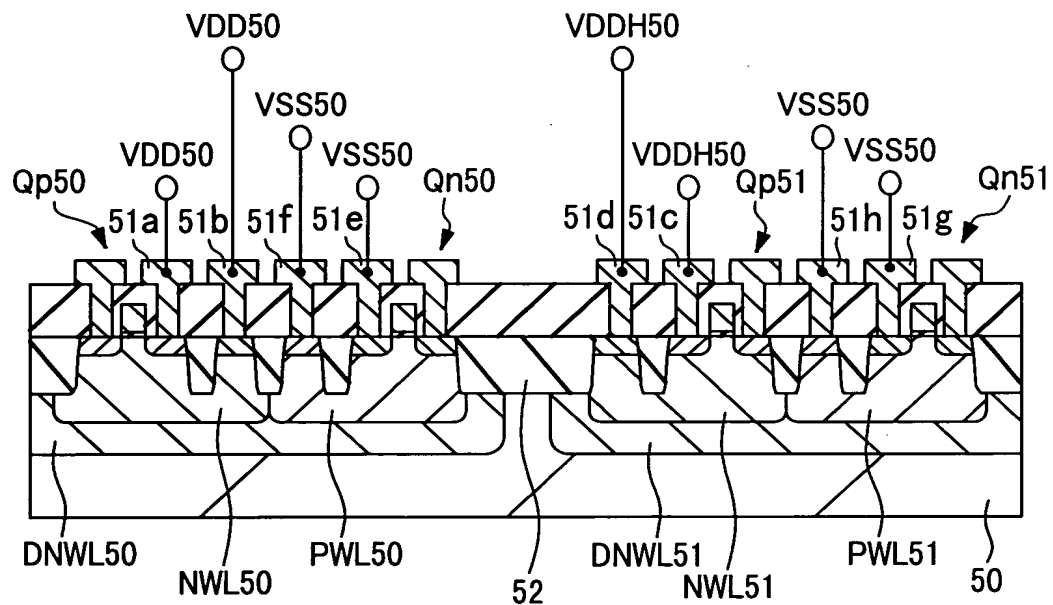


FIG.4



A detailed cross-sectional view of a semiconductor device, likely a memory array or logic circuit. The diagram shows a series of transistors (labeled Qn1, Qp1, Qp2, Qn2) stacked vertically. Each transistor has a gate stack (8g, 8f, 8h1, 8b, 8a, 8c, 8d, 8e, 8h2, 8i, 8j) and a channel region (9). The gates are connected to various voltage sources: VBN=VSSL, VSS, VDD, VDD(OR VDDH), and VSS. The transistors are separated by isolation regions (7a). Below the transistors, there are several horizontal layers: a polysilicon layer (PWL1), a nitride layer (NWL), and a polysilicon layer (PWL2). The entire structure is supported by a substrate (1S). Other labels include 5L, 5, 10a, 12a, 12b, 13a1, 13a2, 2a, 2b, 3, and 4, which refer to specific structural features and layers.

FIG.7

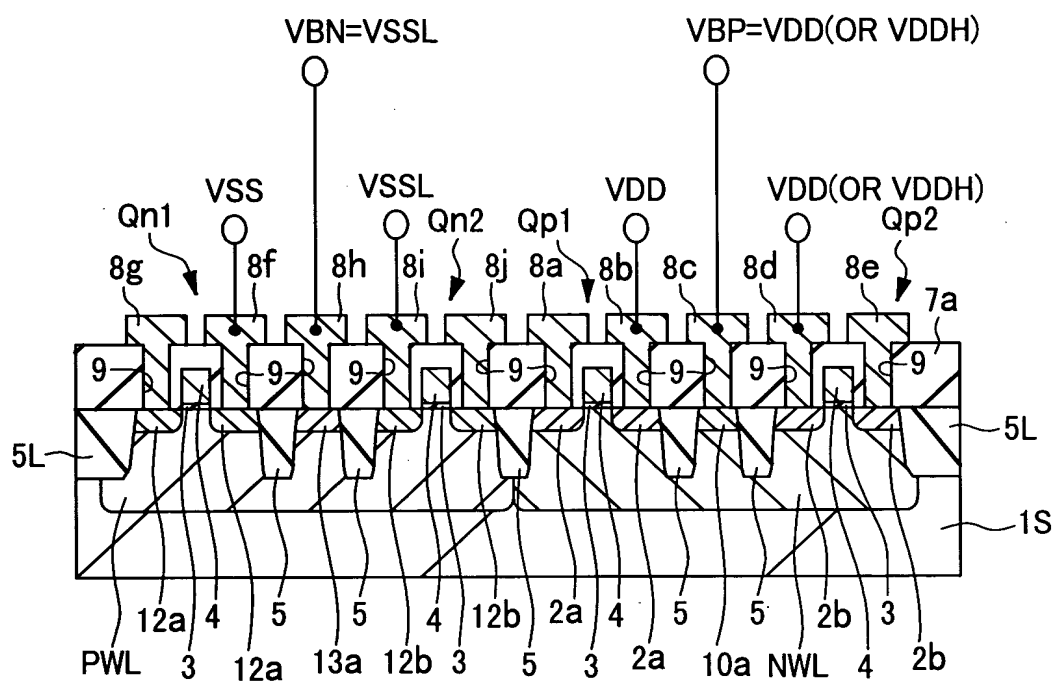


FIG.8

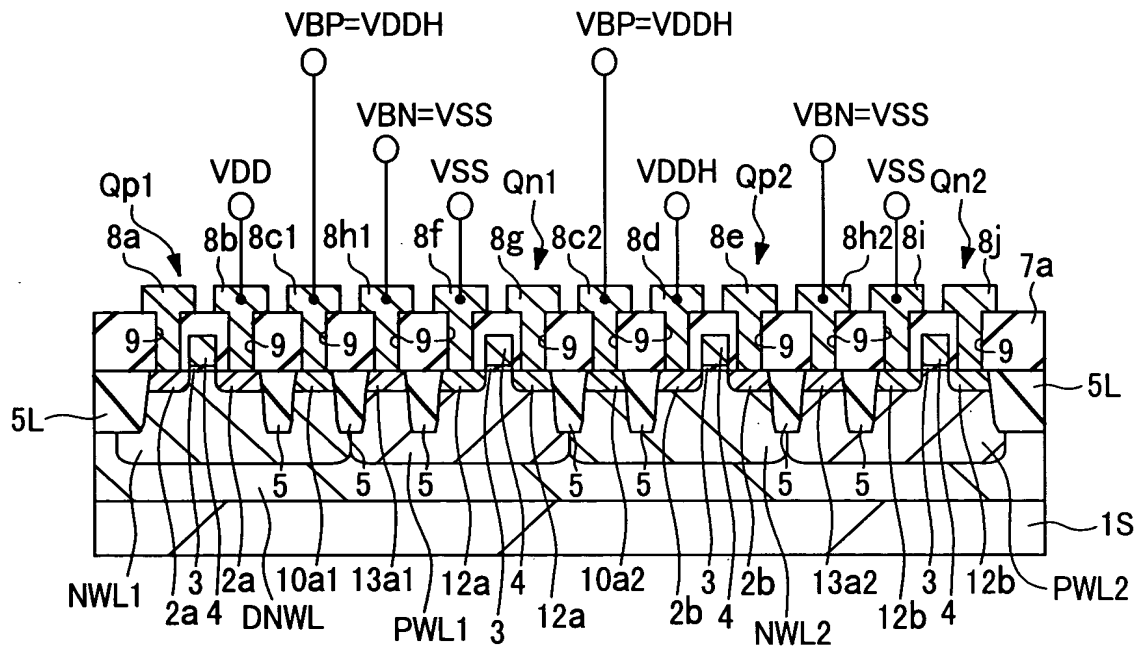


FIG.9

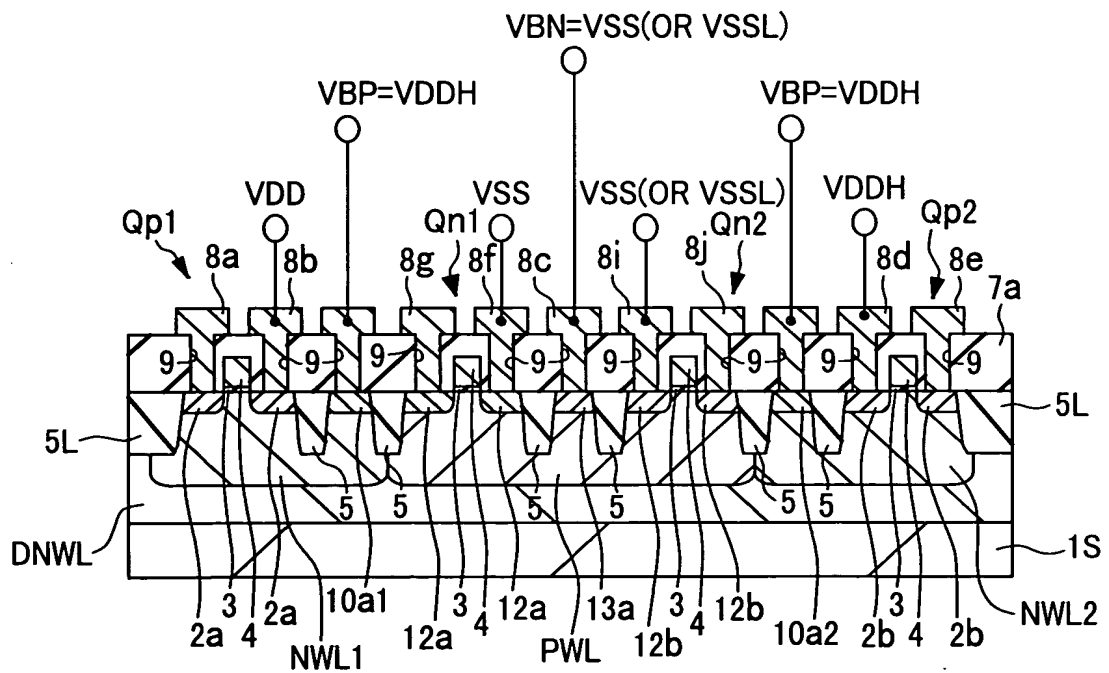


FIG.10

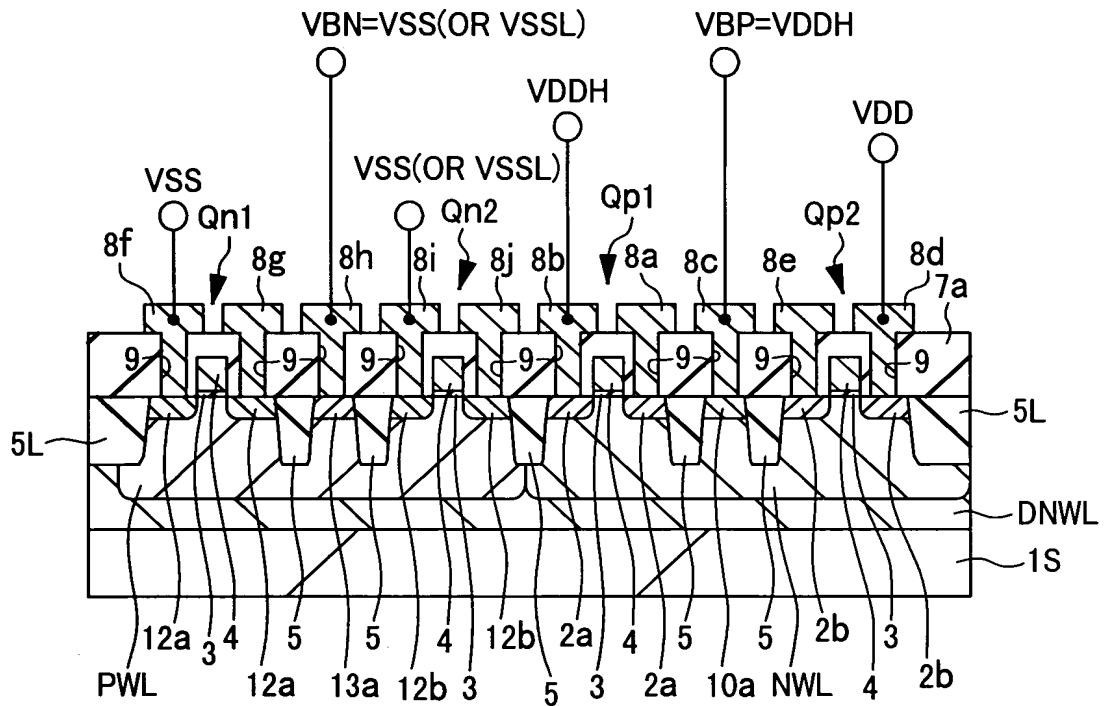


FIG.11

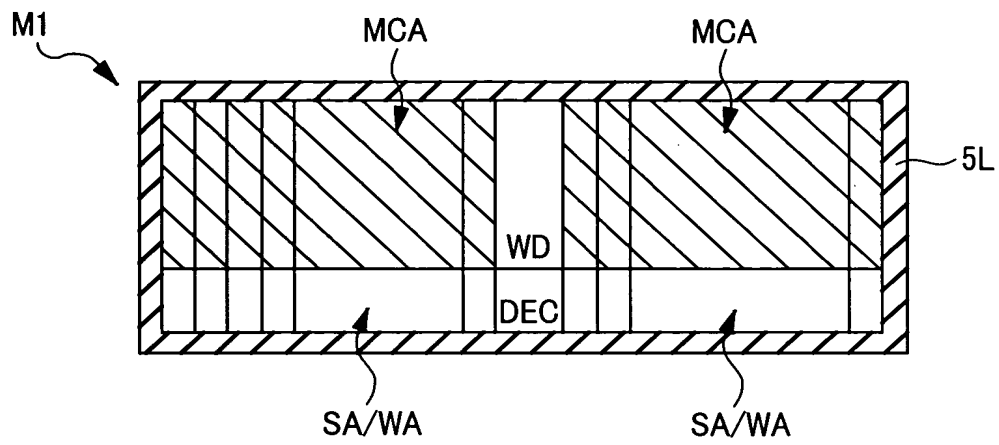


FIG.12

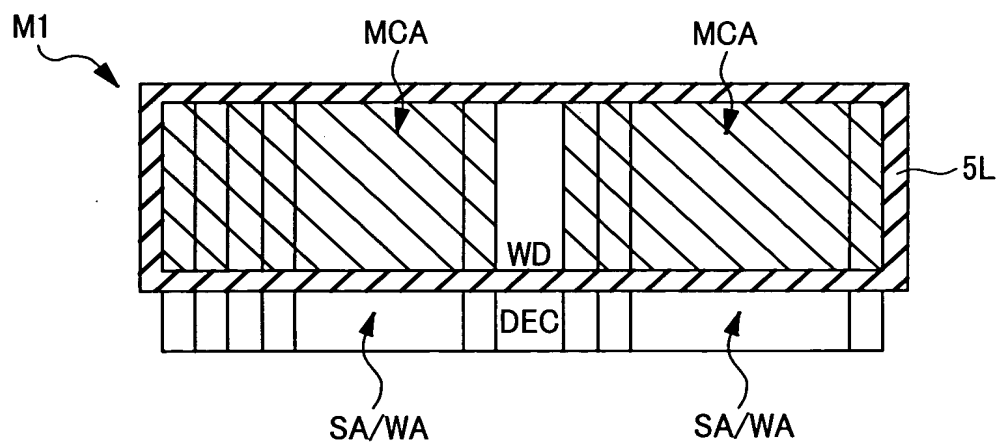


Figure 500 is a cross-sectional view of a semiconductor device. The device features a substrate 501 with a central well region 502. The well region 502 is defined by a width (WD) and is surrounded by a doped region 503. The doped region 503 is formed by a process labeled SA/WA. The top surface of the device is covered by a layer 504, which is also formed by a process labeled SA/WA. The layer 504 is patterned into a series of rectangular blocks, with a central block labeled M50. The blocks are separated by narrow gaps, and the entire structure is labeled MCA.

FIG.15

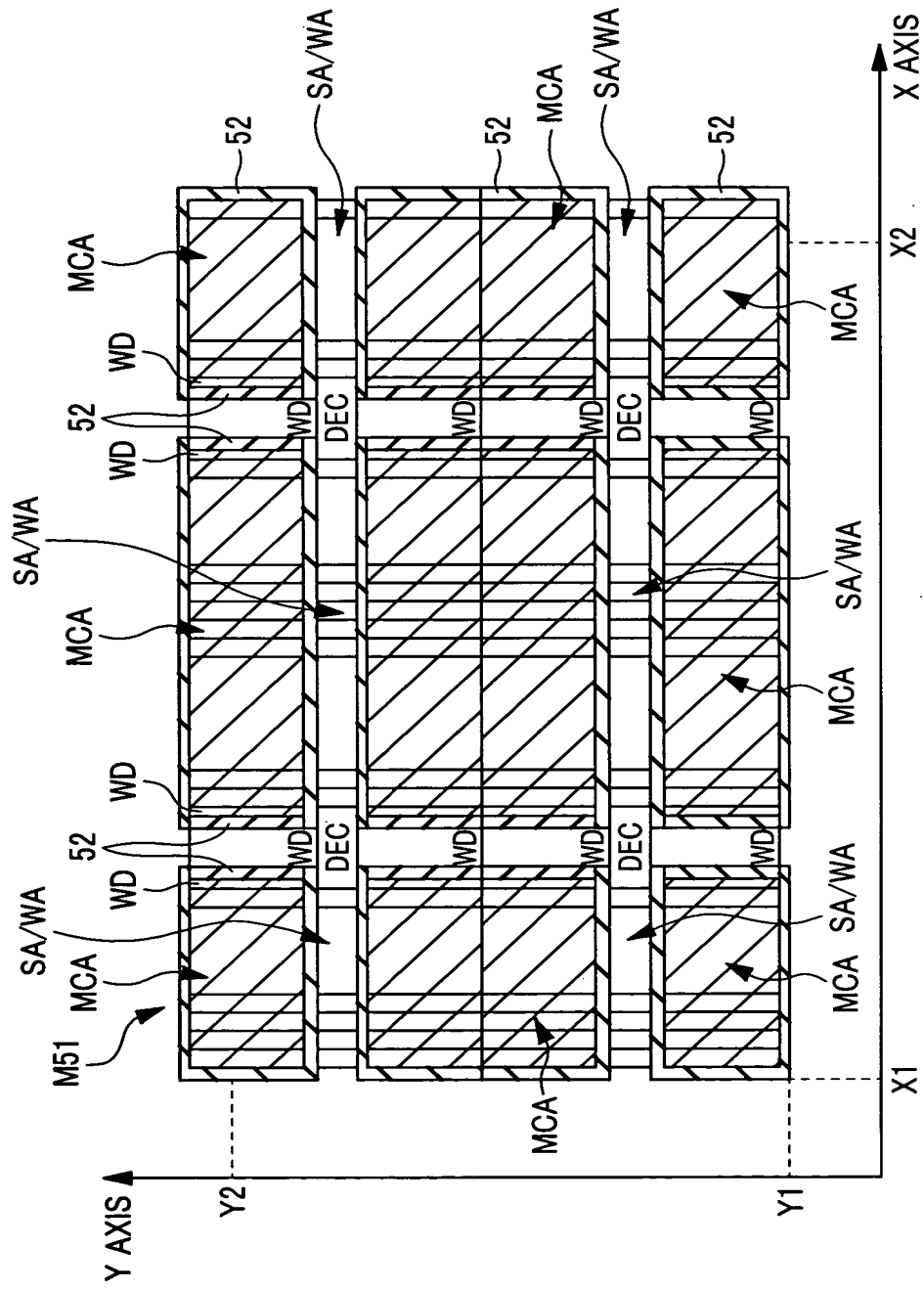


FIG.16

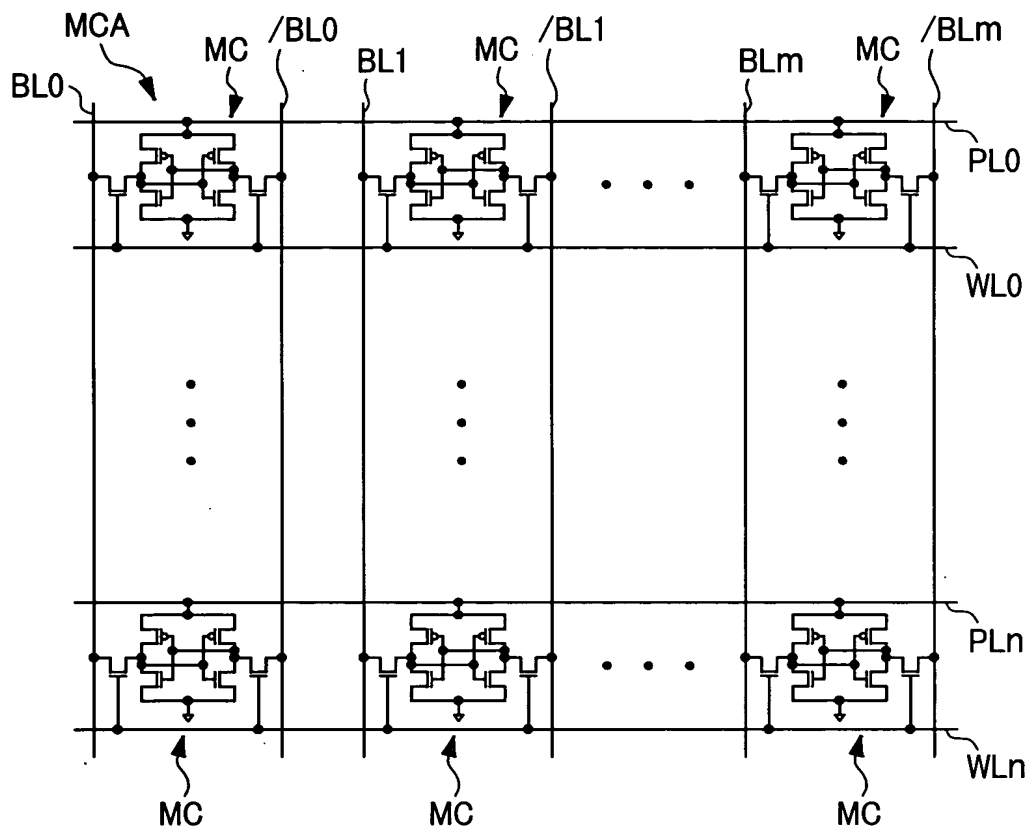


FIG.17

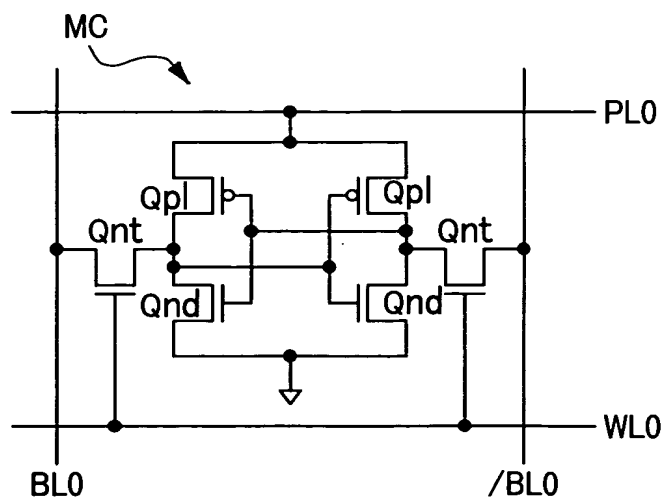


FIG.18

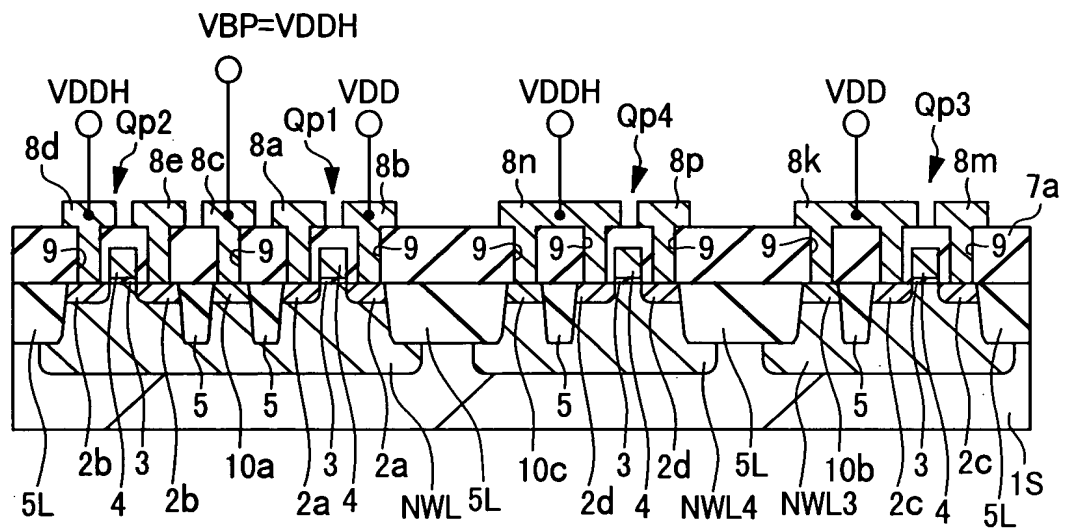


FIG.19

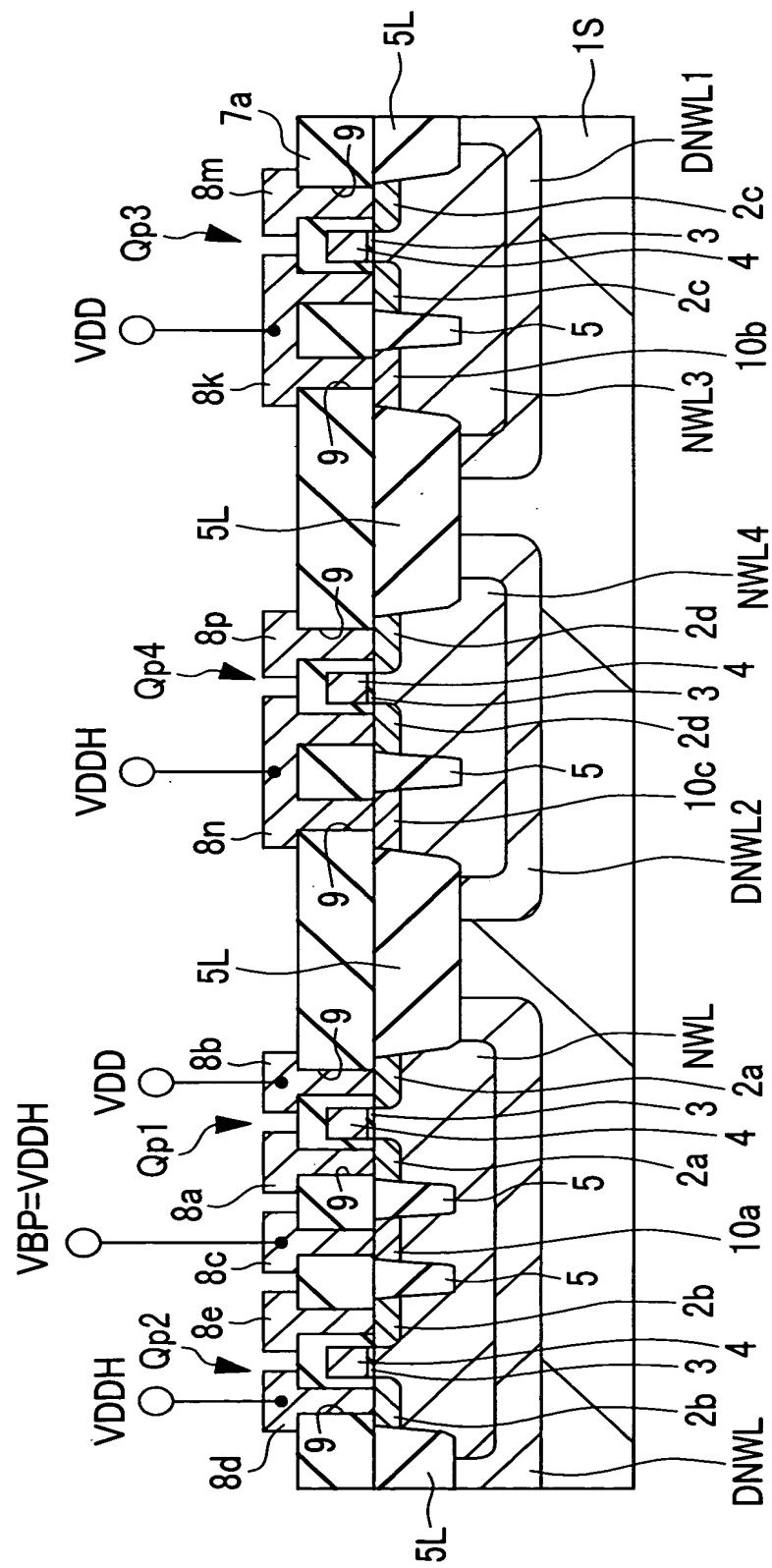


FIG.20

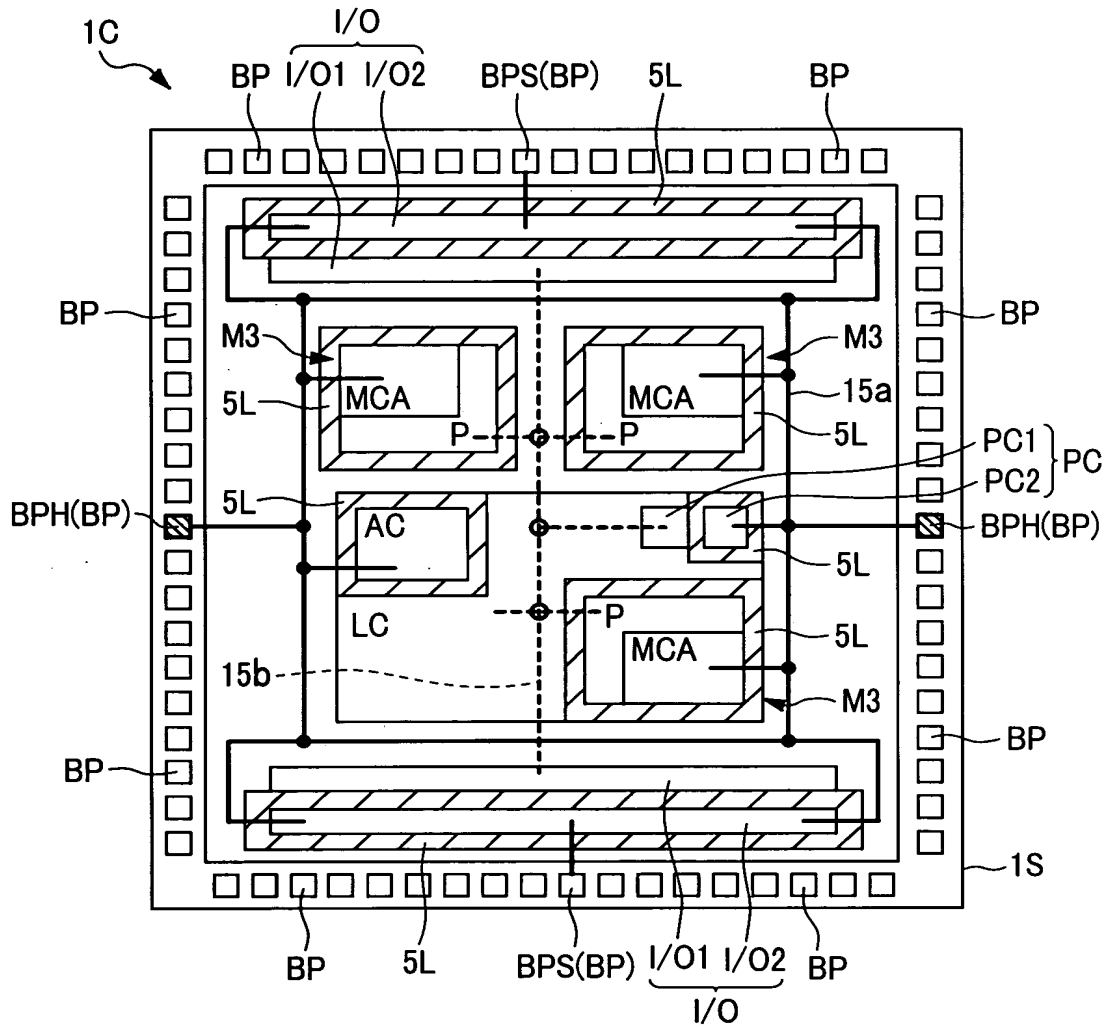


FIG.21

